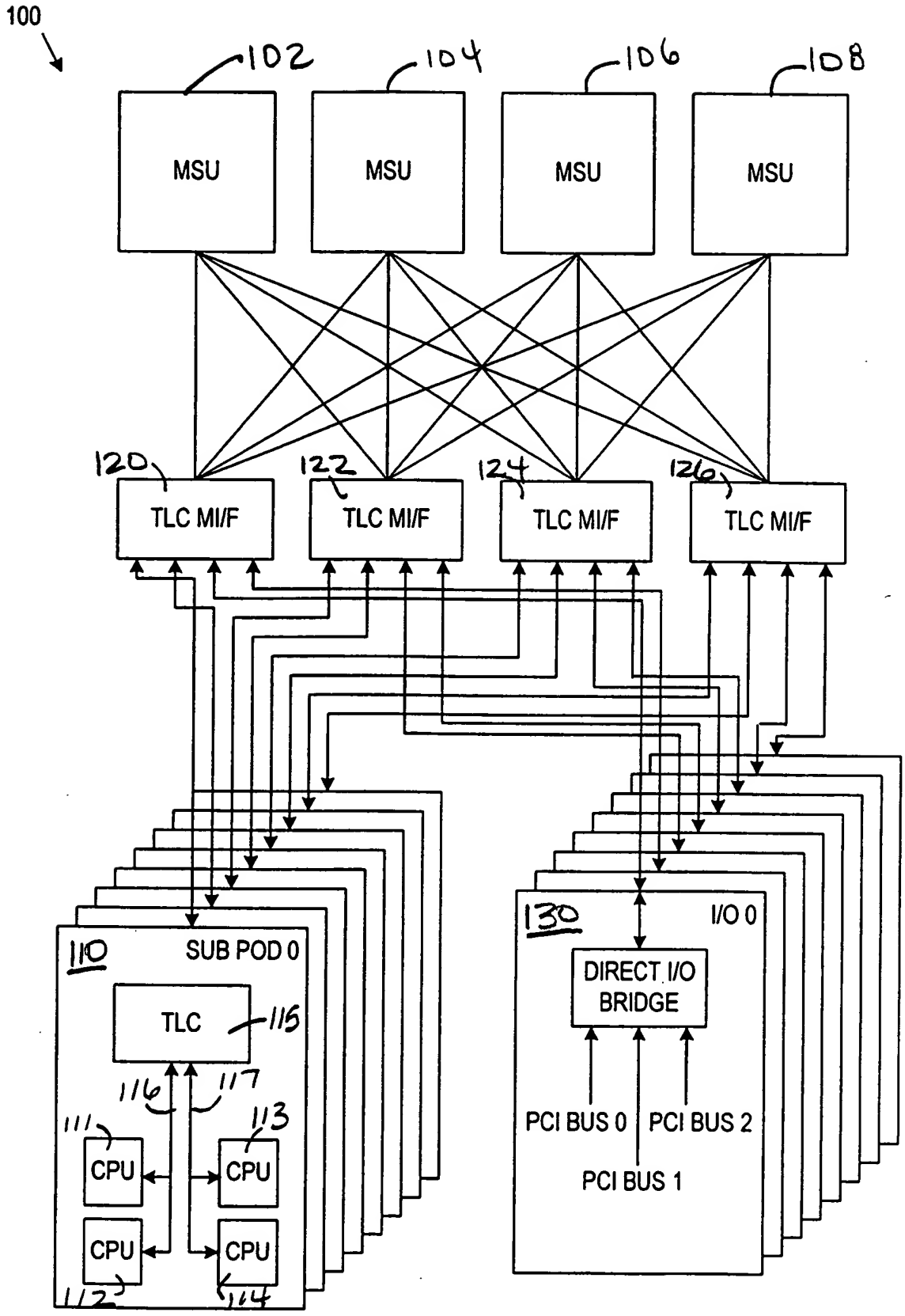
100
102
104
106
108
MSU
MSU
MSU
MSU
120
122
124
126
TLC MI/F
TLC MI/F
TLC MI/F
TLC MI/F
110
SUB POD 0
TLC
115
116
117
111
113
CPU
CPU
CPU
CPU
112
114
130
I/O 0
DIRECT I/O BRIDGE
PCI BUS 0
PCI BUS 2
PCI BUS 1

FIG. 1

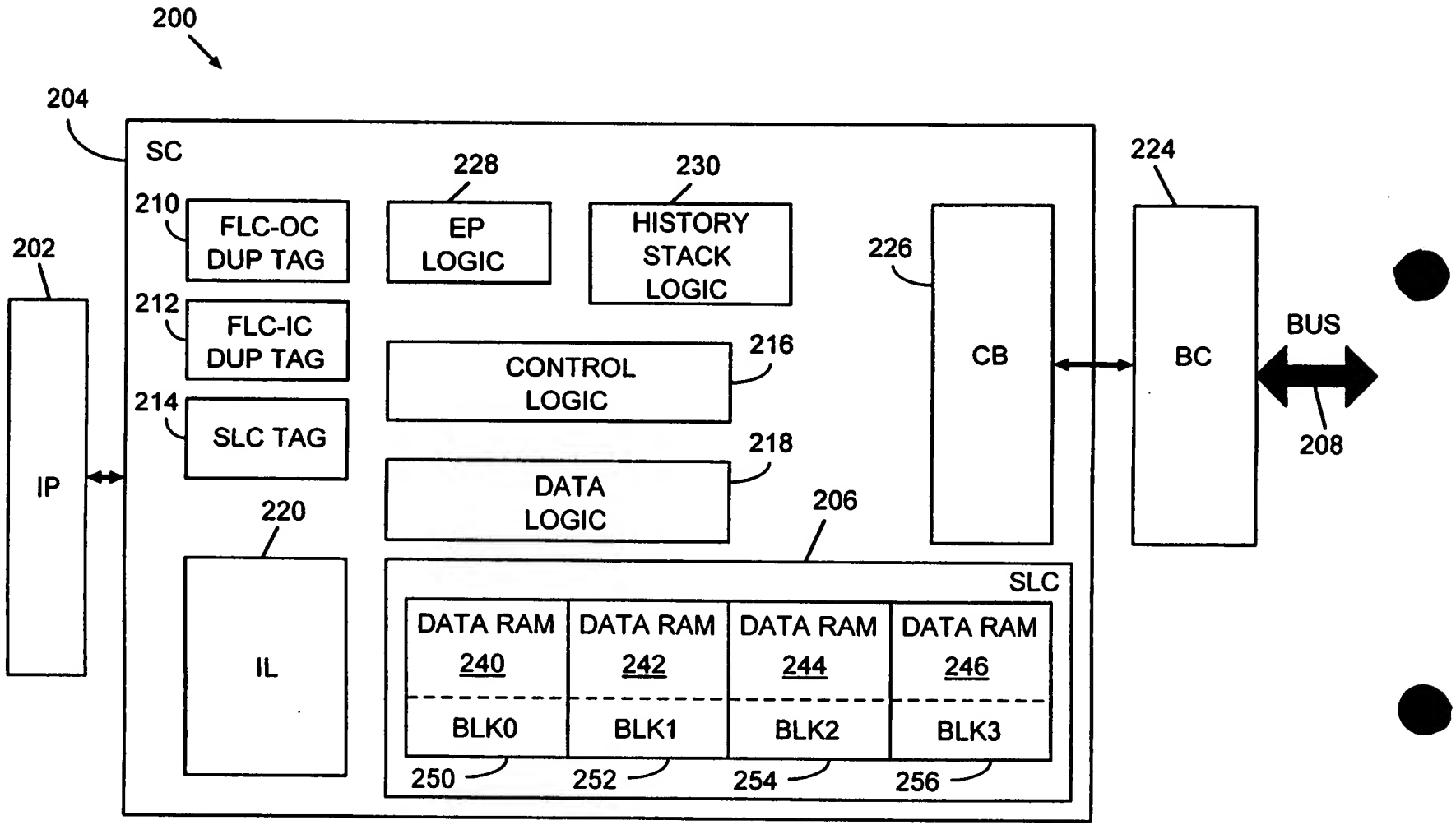
200
204
SC
210
FLC-OC DUP TAG
212
FLC-IC DUP TAG
214
SLC TAG
220
IL
228
EP LOGIC
230
HISTORY STACK LOGIC
216
CONTROL LOGIC
218
DATA LOGIC
206
SLC
DATA RAM 240
DATA RAM 242
DATA RAM 244
DATA RAM 246
BLK0
BLK1
BLK2
BLK3
250
252
254
256
202
IP
226
CB
224
BC
BUS
208

FIG. 2

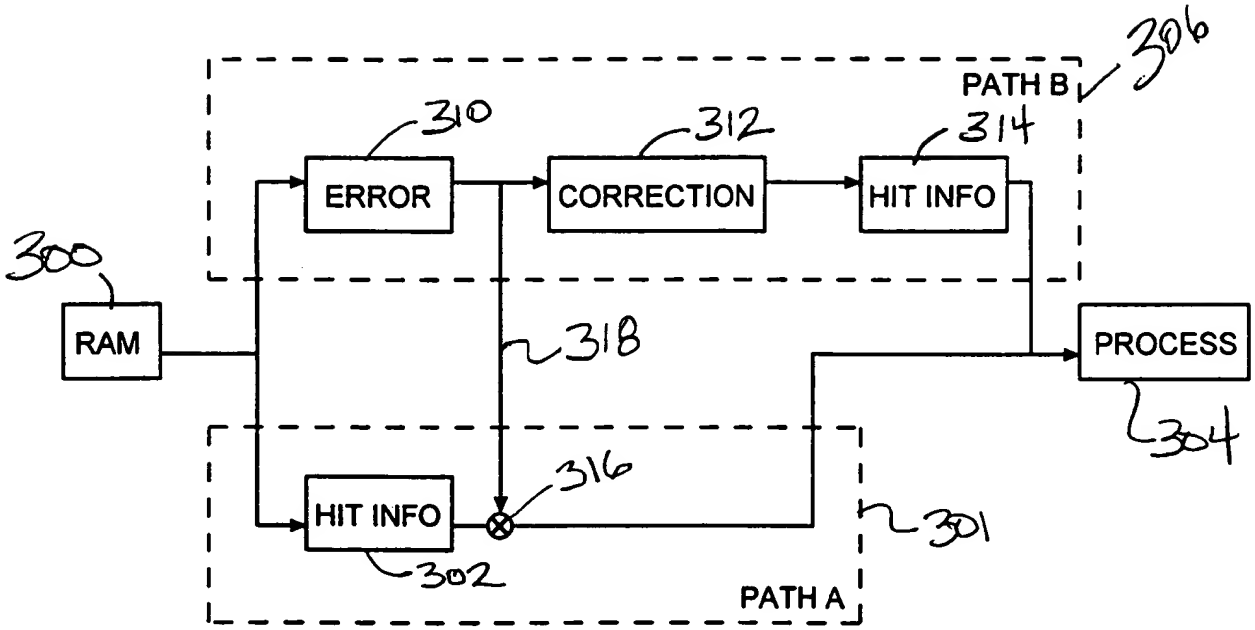
306
PATH B
310
312
314
ERROR
CORRECTION
HIT INFO
300
RAM
318
PROCESS
304
316
HIT INFO
302
301
PATH A

FIG. 3

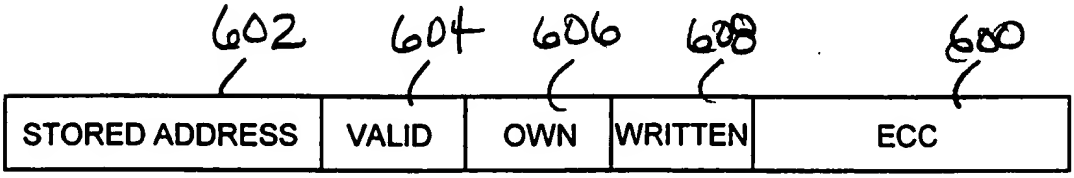
602
604
606
608
600
STORED ADDRESS
VALID
OWN
WRITTEN
ECC

FIG. 6

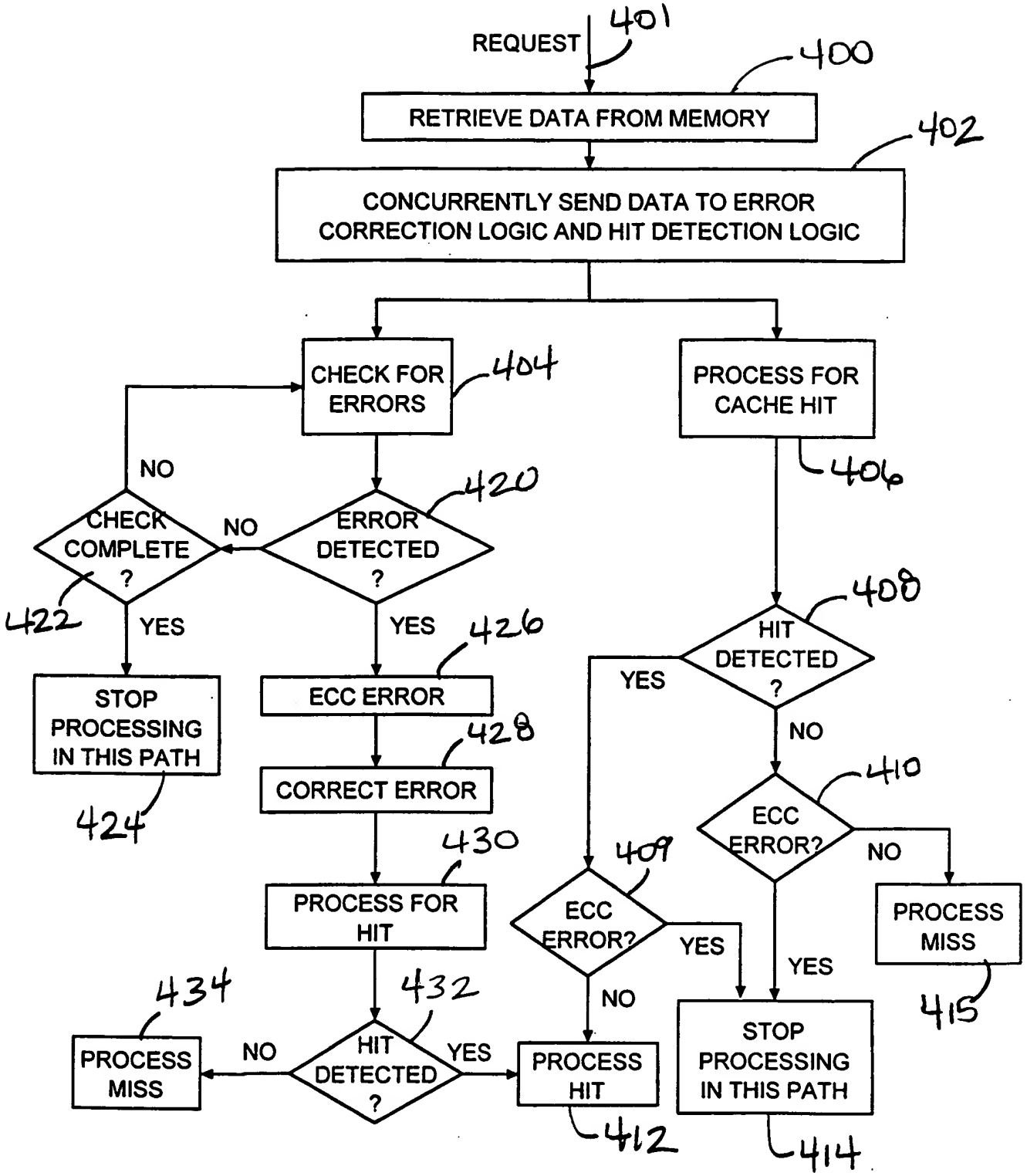
REQUEST
401
400
RETRIEVE DATA FROM MEMORY
402
CONCURRENTLY SEND DATA TO ERROR CORRECTION LOGIC AND HIT DETECTION LOGIC
CHECK FOR ERRORS
404
PROCESS FOR CACHE HIT
406
NO
CHECK COMPLETE ?
NO
ERROR DETECTED ?
420
422
YES
YES
426
STOP PROCESSING IN THIS PATH
424
ECC ERROR
428
CORRECT ERROR
430
PROCESS FOR HIT
432
434
PROCESS MISS
NO
HIT DETECTED ?
YES
PROCESS HIT
412
HIT DETECTED ?
408
YES
NO
409
ECC ERROR?
410
ECC ERROR?
NO
YES
YES
NO
PROCESS MISS
415
STOP PROCESSING IN THIS PATH
414

FIG. 4

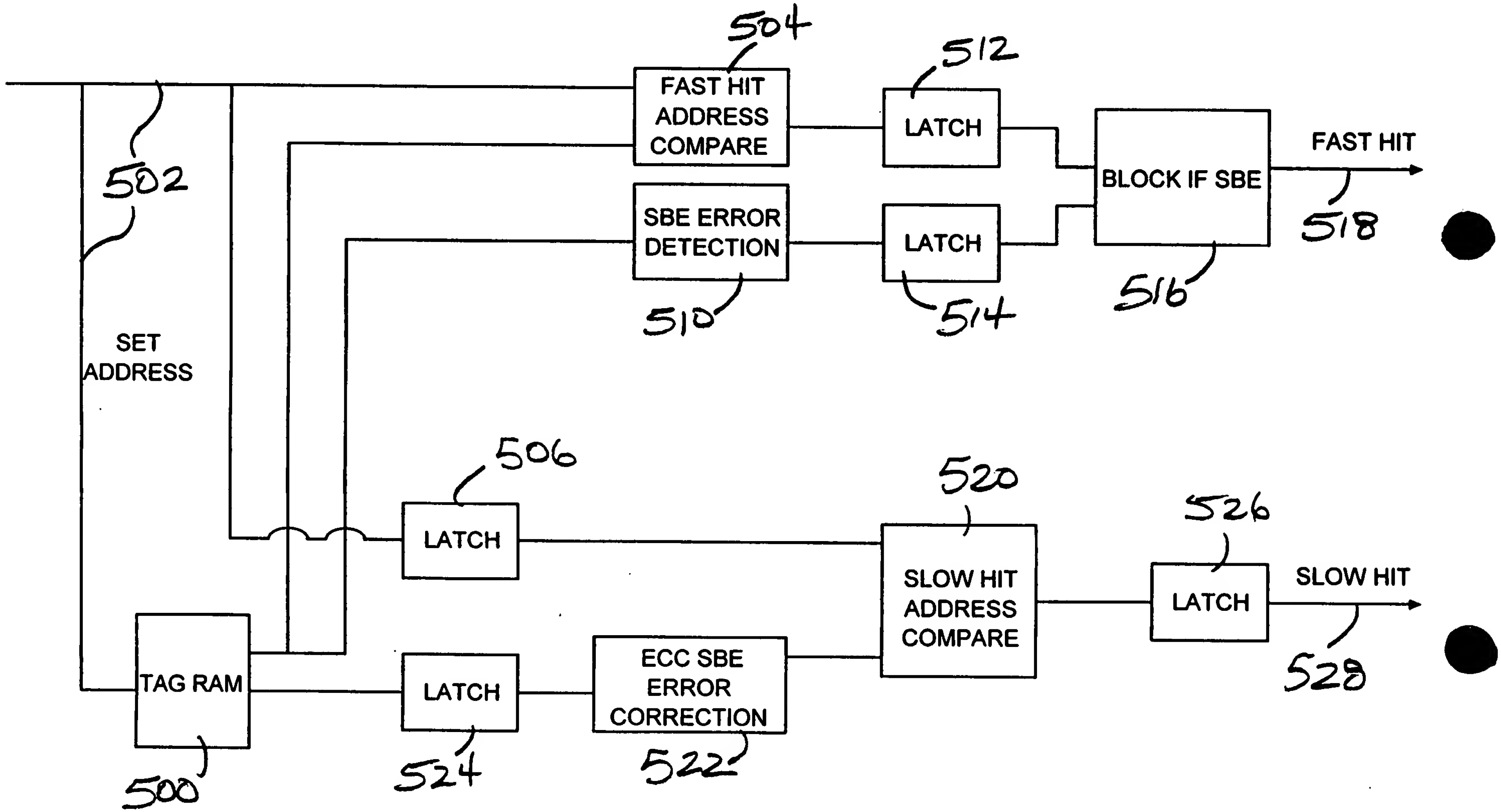
FAST HIT
ADDRESS
COMPARE
504
LATCH
512
BLOCK IF SBE
516
FAST HIT
518
SBE ERROR
DETECTION
510
LATCH
514
502
SET
ADDRESS
LATCH
506
SLOW HIT
ADDRESS
COMPARE
520
LATCH
526
SLOW HIT
528
TAG RAM
500
LATCH
524
ECC SBE
ERROR
CORRECTION
522

FIG. 5